UCC3585 Low-Voltage Synchronous-Buck Converter Evaluation Board UCC3585EVM–014

Christopher Bridge *Power Supply Control Products*

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1 Introduction

This user's guide details the Texas Instruments (TI) UCC3585EVM–014 (SLUP014) low-voltage synchronous-buck evaluation module (EVM). It includes a list of EVM features, specifications, schematics, operating guidelines, bill of materials, and experimental results.

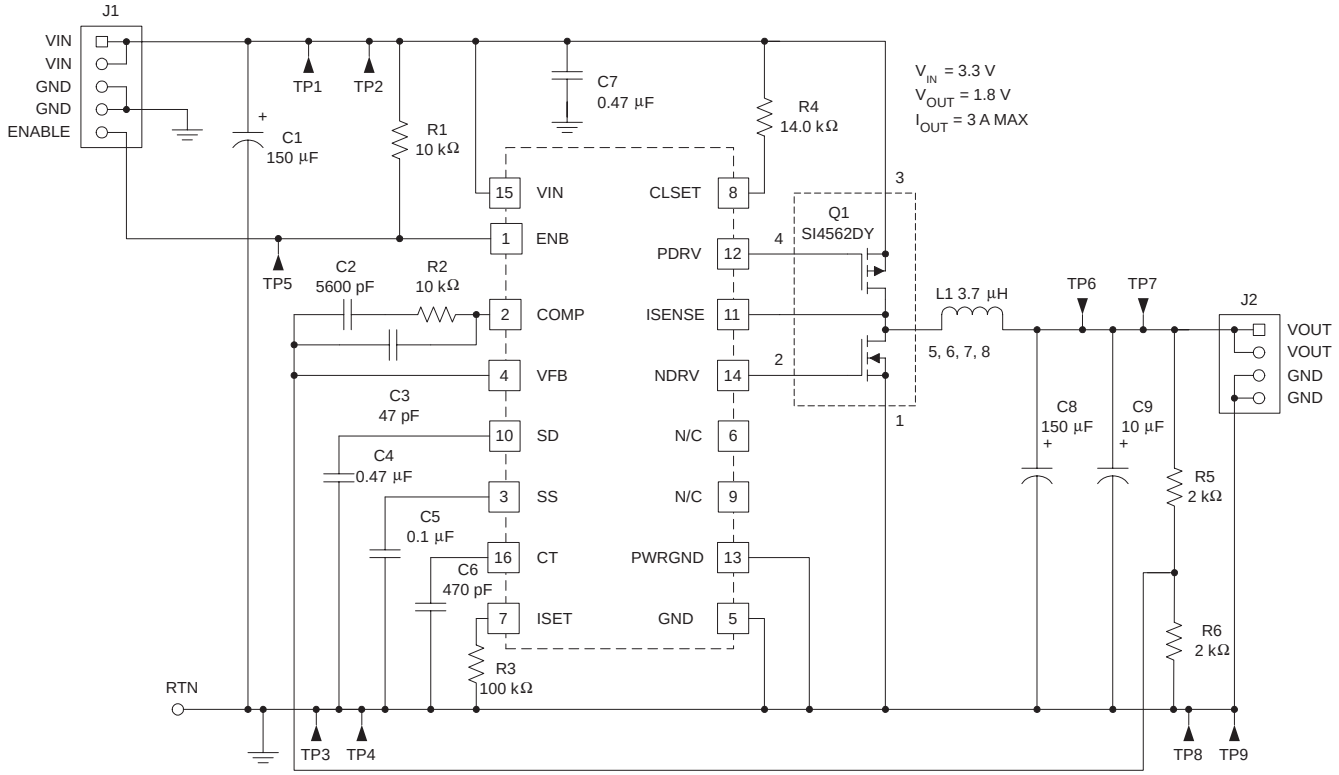
1.1 Features

- Converts a 3.3-V ±10% Input to a 1.8-V Output at up to 3-A Load Current
- Greater than 2% Output Voltage Accuracy
- High-Efficiency Synchronous Power Conversion Using P-Channel High-Side and N-Channel Low-Side MOSFETs
- Sophisticated Programmable Current Limiting Using the P-Channel $R_{DS(on)}$
- Logic-Compatible Shutdown with Low-Quiescent Current Off-State
- Output Voltage Programmable Down to 0.9 V

1.2 Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	I_{LOAD} = 0 A to 3 A	3	3.3	3.6	V
Output voltage	I_{LOAD} = 1 A, VIN = 3.3 V, T_A = 25°C	1.764	1.800	1.836	V
Current limit inception point	VIN = 3.3 V	3			A
Full load efficiency	VIN = 3.3 V, I_{LOAD} = 3 A		87%		
Minimum load	3.0 V ≤ VIN ≤ 3.6	0			A
Maximum load	3.0 V ≤ VIN ≤ 3.6	3.0			A
Switching frequency	VIN = 3.3 V		300		kHz

1.3 Schematic



UDG–00163

Figure 1. Evaluation Module Schematic

2 Operating Guidelines

2.1 Input and Output Connections

Referring to the UCC3585EVM–014 schematic (Figure 1), there are two pin headers to connect input power and output load to the PCB. Input power is supplied to J1, and output loads are connected to J2. Both J1 and J2 have two pins each for connecting ground and input or output. These two pins allow Kelvin sensing of the actual input and output voltages at the PCB board level, eliminating any contact and lead resistances. Figure 2 shows a typical connection using Kelvin connections and an input power supply with remote sensing.

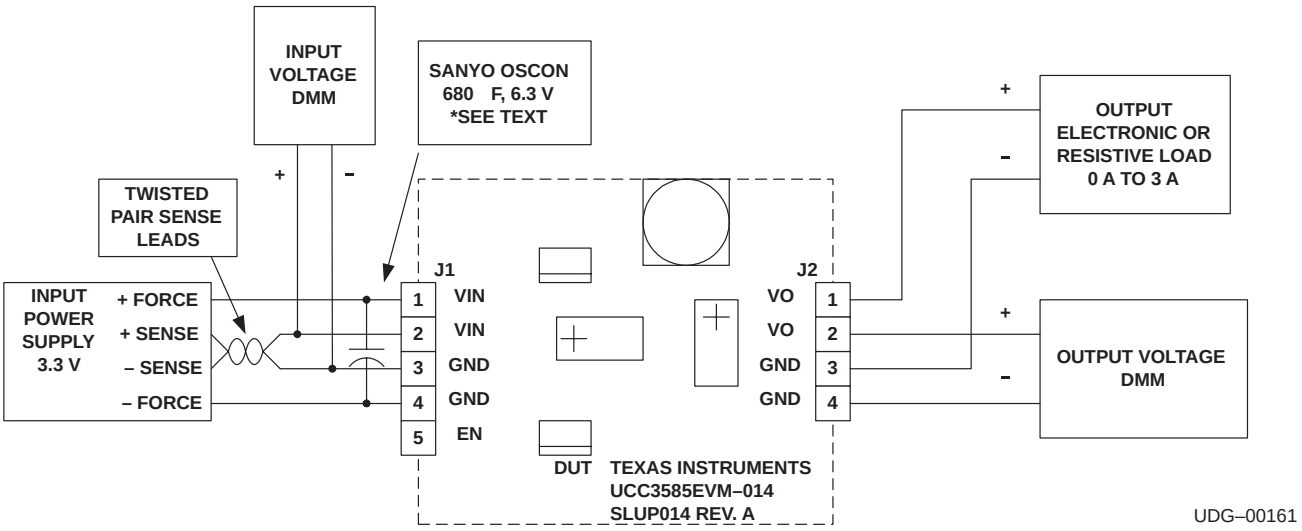


Figure 2. Kelvin Sensing

Some bench power supplies oscillate when the remote sensing feature is used, particularly when the load is a switch–mode power supply like the UCC3585EVM–014. There are two possible remedies for stabilizing the input supply, first, by placing a large capacitance value electrolytic capacitor across the force inputs at the EVM, and secondly, twisting or shielding the sense leads. If these methods fail to correct the oscillation, the EVM should be powered without Kelvin sensing as shown in Figure 3.

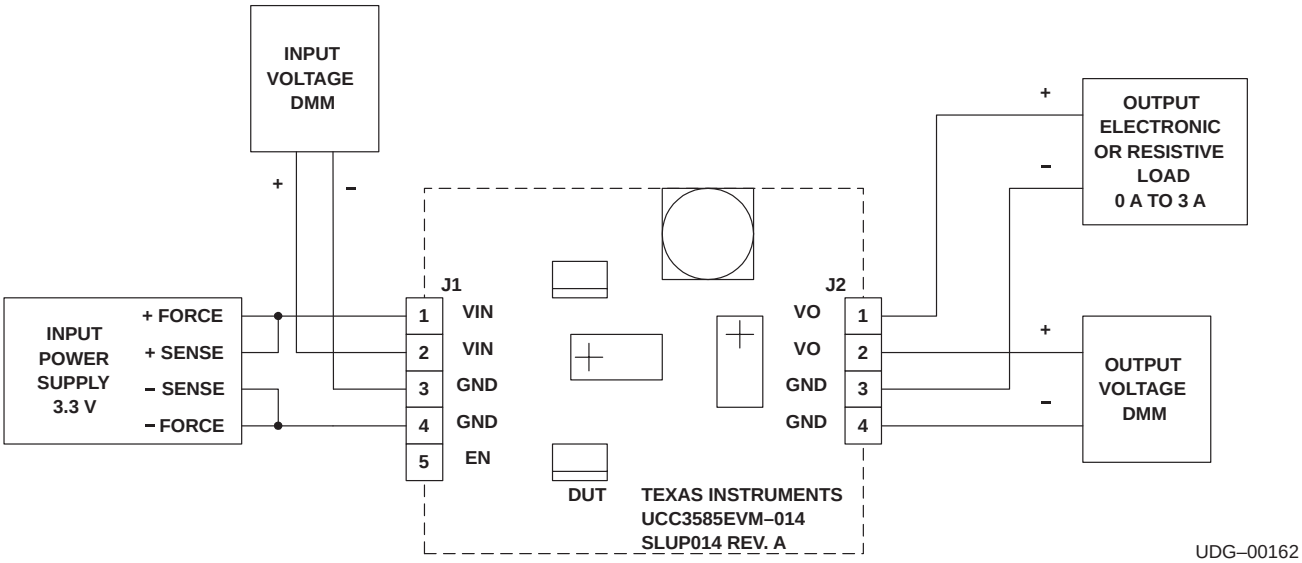


Figure 3. No Kelvin Sensing

2.2 Enable Input

The UCC3585EVM–014 has an enable connection on Pin 5 of J1. An on-board pull-up resistor puts the UCC3585 into an enabled state. To disable the UCC3585, the EN pin can be either pulled low by an open-collector or open-drain transistor, or driven with a gate powered from the input voltage rail. In either case, the EN pin must be driven high to the input voltage rail to turn the UCC3585 IC on.

3 Evaluation Module Layouts

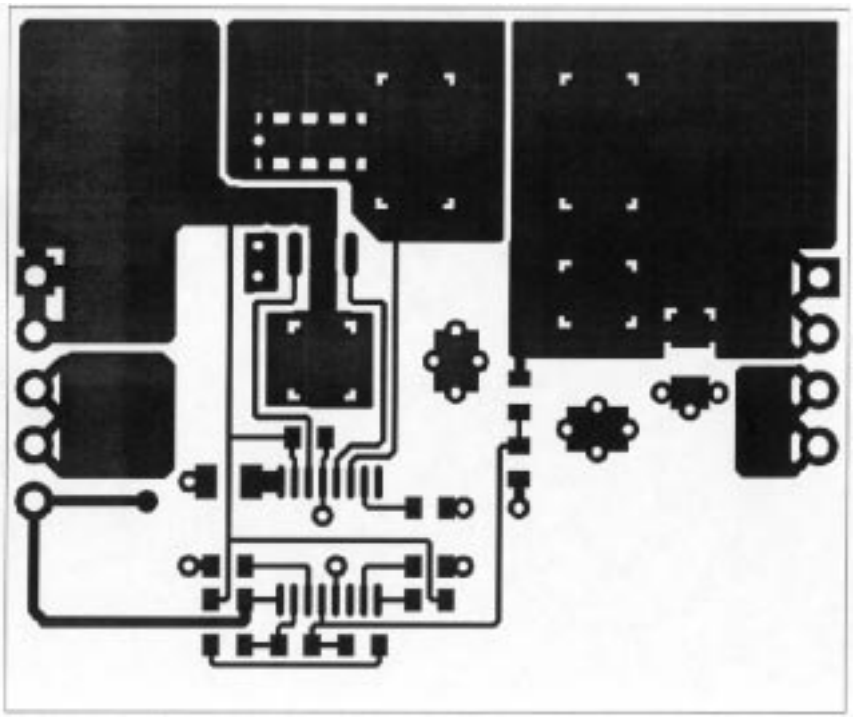


Figure 4. Top Layer (top view)

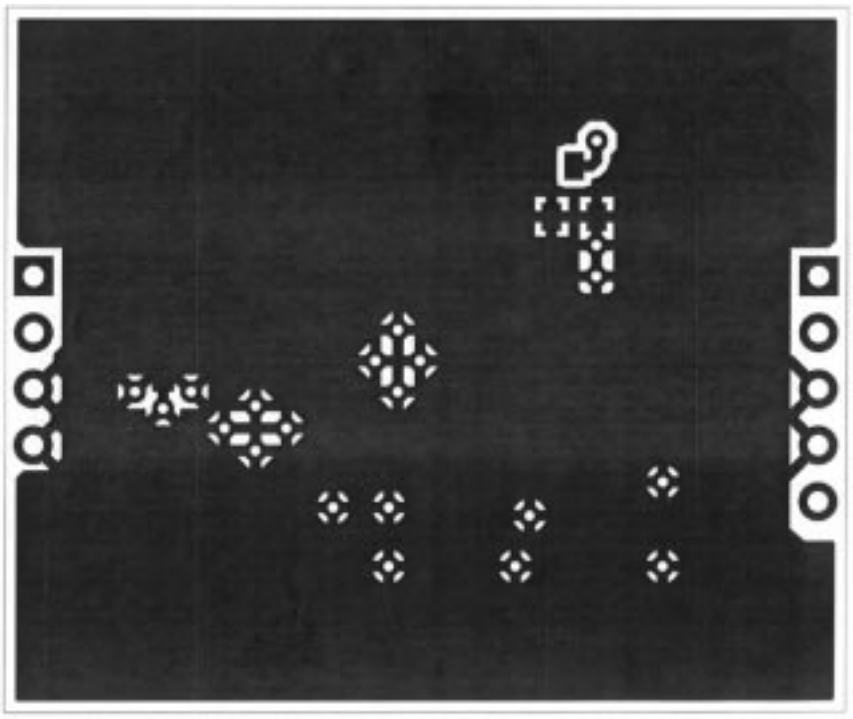


Figure 5. Bottom Layer (bottom view)

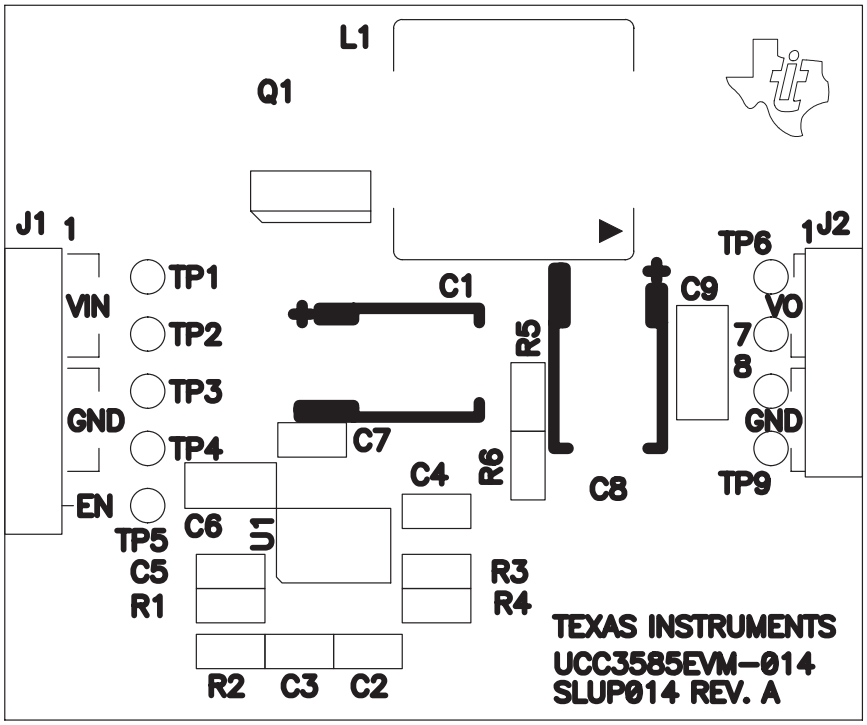


Figure 6. Top Layer (top view)

4 Bill of Materials

Reference	Qty	Part Number	Description	MFG
C1, C8	2	6TPB150M	Capacitor, Poscap, 150 μF, 6.3 V, 20%	Sanyo
C2	1	ECJ–1VB1H562K	Capacitor, Ceramic, 5600 pF, 50 V, 10%, X7R	Panasonic
C3	1	ECJ–1VC1H470J	Capacitor, Ceramic, 47 pF, 50 V, 5%, NPO	Panasonic
C4, C7	2	ECJ–1VB0J474K	Capacitor, Ceramic, 0.47 μF, 6.3 V, 10%, X5R	Panasonic
C5	1	ECJ–1VB1C104K	Capacitor, Ceramic, 0.1 μF, 16 V, 10%, X7R	Panasonic
C6	1	ECJ–2VC1H471J	Capacitor, Ceramic, 470 pF, 50 V, 5%, NPO	Panasonic
C9	1	JMK316BJ106ML	Capacitor, 10 μF, 6.3V, 10%, X5R	Taiyo–Yuden
D1	0	ZHCS1000	Diode, Schottky, SOT23, 1 A	Zetex
J1	1 per 8	800–10–064–10–001	Header, 64-pin strip, cut to 5 pins per assembly, Gold Plate, 0.024 inch tail, 0.030 inch pin (0.028 inch hole)	Mill–Max
J2	1 per 8	800–10–064–10–001	Header, 64-pin strip, cut to 4 pins per assembly, Gold Plate, 0.024 inch tail, 0.030 inch pin (0.028 inch hole)	Mill–Max
J1 mate	1 per 8	801–93–050–10–001	Header, 50-pin strip, cut to 5 sockets per assembly, Gold Plate, 0.024 inch tail, 0.030 inch pin (0.028 inch hole)	Mill–Max
J2 mate	1 per 8	801–93–050–10–001	Header, 50-pin strip, cut to 4 sockets per assembly, Gold Plate, 0.024 inch tail, 0.030 inch pin (0.028 inch hole)	Mill–Max
L1	1	919AS–3R7	Inductor, 3.7 μH, Toko or	Toko
L1–alt	0	CDRH104R–3R8	Inductor, 3.8 μH, Sumida	Sumida
Q1	1	Si4562DY	MOSFET, N–channel/ P–chhannel SOIC–8	Siliconix
R1, R2	2	ERJ–3EKF1002	Resistor, Chip, 10.0 kΩ, 1/16W, 1%	Panasonic
R3	1	ERJ–3EKF1003	Resistor, Chip, 100 Ω, 1/16W, 1%	Panasonic
R4	1	ERJ–3EKF1402	Resistor, Chip, 14.0 kΩ, 1/16W, 1%	Panasonic
R5, R6	2	ERJ–3EKF2001	Resistor, Chip, 2.00 kΩ, 1/16W, 1%	Panasonic
U1	1	UCC3585M	Controller IC, QSOP package	TI
–	–	PCB	PCB description	any

5 Typical Performance

Figure 7 shows the typical efficiency of the EVM. Data were taken at 3.3-V input and at room temperature using pulsed measurements.

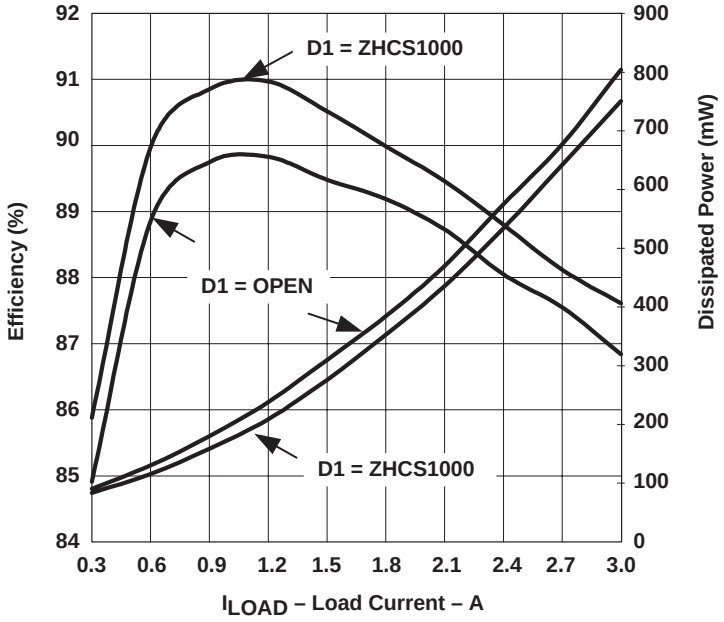


Figure 7. Efficiency and Dissipated Power vs. Load Current

Figure 8 shows the switching frequency output ripple at J2. The output ripple was measured with 20-MHz bandwidth limiting and ac coupled.

Figure 9 shows the transient response due to a step-load change from 1 A to 2 A (1-A peak step change). The sampling is averaged to eliminate the switching frequency ripple from the waveforms.

SWITCHING FREQUENCY OUTPUT RIPPLE AT J2

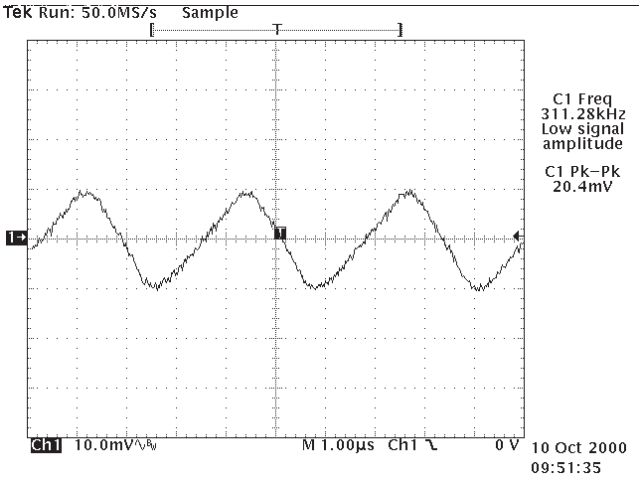


Figure 8

TRANSIENT RESPONSE DUE TO STEP LOAD CHANGE

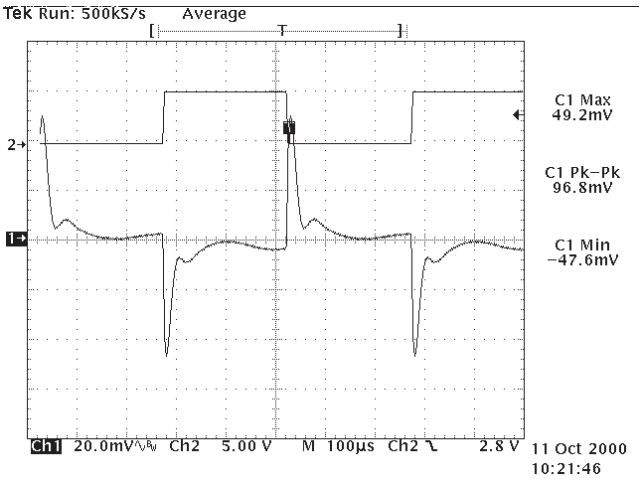


Figure 9

6 References

1. UCC3585, *Low-Voltage Synchronous-Buck Converter*, Texas Instruments Datasheet, revised 2000, Literature No. SLUS304.

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